

S/N 10/023,819

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Biju Chandran et al.	Examiner:	John Vigushin
Serial No.:	10/023,819	Group Art Unit:	2827
Filed:	December 21, 2001	Docket:	884.A27US1
Title:	CHIP-JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN THE ADHERENTS AND SEMICONDUCTOR PACKAGE MADE THEREBY		
Assignee:	Intel Corporation	Customer No:	21186

INFORMATION DISCLOSURE STATEMENT

U.S. Patent and Trademark Office
220 20th Street South, Customer Window, **Mail Stop 313(c)**
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

BIJU CHANDRAN ET AL.

By their Representatives,

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Date Oct. 21, 2004

By Ann M. McCrackin
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Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being hand-delivered to: U.S. Patent and Trademark Office, 220 20th Street South, Customer Window, **Mail Stop 313(c)**, Crystal Plaza Two, Lobby, Room 1B03, Arlington, VA 22202, on this 22nd day of October, 2004.

Jennifer Flynn
Name

[Signature]
Signature

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Application Number</td> <td>10/023,819</td> </tr> <tr> <td>Filing Date</td> <td>December 21, 2001</td> </tr> <tr> <td>First Named Inventor</td> <td>Chandran, Biju</td> </tr> <tr> <td>Group Art Unit</td> <td>2827</td> </tr> <tr> <td>Examiner Name</td> <td>Vigushin, John</td> </tr> </table>	Application Number	10/023,819	Filing Date	December 21, 2001	First Named Inventor	Chandran, Biju	Group Art Unit	2827	Examiner Name	Vigushin, John
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Group Art Unit	2827										
Examiner Name	Vigushin, John										
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US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		HONG, B. Z., "Thermal Fatigue Analysis of CBGA Package with Lead-Free Solder Fillets", <u>Proceedings of the 1998 Intersociety Conference on Thermal Phenomena</u> , (Aug., 1998),205-211	
		KARIM, Z. S., et al., "Lead-Free Bump Interconnections for Flip-Chip Applications", <u>Proceedings of the 2000 IEEE/CPMT International Electronics Manufacturing Technology Symposium</u> , (Jan., 2000),274-278	
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		XIAO, G. , et al., "The Effect of Cu Stud Structure and Eutectic Solder Electroplating on Intermetallic Growth and Reliability of Flip-Chip Solder Bump", <u>Proceedings of the 2000 Electronic Components and Technology Conference</u> , (Sep., 2000),54-59	

EXAMINER

DATE CONSIDERED